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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,960	04/13/2004	Pey-Yuan Lee	24061.187 (2003-1398)	3594
42717	7590	03/09/2006	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			HUYNH, ANDY	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/822,960

Applicant(s)

LEE ET AL.

Examiner

Andy Huynh

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-9 and 23-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7-9 is/are allowed.
- 6) ☒ Claim(s) 1,2,4-6 and 23-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

In the Amendment dated February 17, 2006, Claims **1 and 2** have been amended.

Response to Arguments

Applicant's arguments with respect to Claims **1, 2, 4-6 and 23-25** have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim **1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh et al. (USP 6,900,135 hereinafter referred to as "Somekh") in view of Shinada et al. (USP 6,329,826 hereinafter referred to as "Shinada").

Somekh discloses in Fig. 1 and the corresponding texts as set forth in column 3, line 40-column 4, line 56, a method of manufacturing a microelectronic device, comprising:

performing a first inspection of a device feature/wafer during an intermediate stage of manufacture;

cleaning the device feature/wafer after the first inspection; and

performing a second inspection of the device feature after cleaning the device feature/wafer, wherein the first and second inspections are performed by a single inspection tool/a buffer station 104 (col. 3, lines 44-45).

Somekh does not disclose a device feature formed on a substrate. Shinada teaches in Figs. 1-2 a circuit pattern inspection method and apparatus comprises a device feature formed on a substrate 9 to be able to detect a defect generated on the circuit pattern in an early stage (col. 11, line 60-col. 12, line 10). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a device feature on a substrate, as taught by Shinada in order to detect a defect generated on the circuit pattern in an early stage, and the percentage of defects in the semiconductor device and other substrates can be reduced so that producing efficiency can be improved (col. 35, lines 1-17).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh et al. (USP 6,900,135 hereinafter referred to as "Somekh") in view of Shinada et al. (USP 6,329,826 hereinafter referred to as "Shinada") and further in view of Pike (USP 6,410,927).

Somekh discloses all the claimed limitations as stated in Claim 1 except for a device feature formed on a substrate, and the first inspection is performed by a first inspection tool and the second inspection is performed by a second inspection tool different than the first inspection tool. Shinada teaches in Figs. 1-2 a circuit pattern inspection method and apparatus comprises a device feature formed on a substrate 9 to be able to detect a defect generated on the circuit pattern in an early stage (col. 11, line 60-col. 12, line 10). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a device feature on a substrate, as taught by Shinada in order to detect a defect generated on the circuit pattern in an early stage, and the percentage of defects in the semiconductor device and other substrates can be reduced so that producing efficiency can be improved (col. 35, lines 1-17). Shinada does not explicitly disclose the first inspection is performed by a first inspection tool and the second inspection is performed by a second inspection tool different than the first inspection tool. Pike teaches that wafers are subject to an initial scan under low magnification using a first inspection tool/an inspection tool and transferred to a second inspection tool/a high magnification analysis tool for more complete analysis in a method for detecting defects in both processed and unprocessed wafers in order to easily find defects when a wafer is transferred from tool to tool as set forth in the Abstract. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to utilize the teachings of using a first inspection tool/an inspection tool for a first process/an initial scan under low magnification and a second inspection tool for a second process/a high magnification analysis tool, as taught by Pike to incorporate into Somekh and Shinada's processes to arrive the claimed limitation in order to easily find defects when a wafer is transferred from tool to tool.

Art Unit: 2818

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh et al. (USP 6,900,135 hereinafter referred to as “Somekh”) in view of Shinada et al. (USP 6,329,826 hereinafter referred to as “Shinada”) and further in view of Iwabuchi et al. (USP 6,512,227 hereinafter referred to as “Iwabuchi”).

Somekh and Shinada disclose all the claimed limitations except for at least one of the first and second inspections performed by a scanning electron microscope (SEM). Iwabuchi teaches that as one of apparatuses for observing a sample with an electron beam, there is known a scanning electron microscope (SEM). The SEM is suitable for observing a by restricted field of vision at a high magnification (col. 1, lines 32-39). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to use at least one of the first and second inspections is performed by a scanning electron microscope (SEM), as taught by Iwabuchi to incorporate into Somekh and Shinada’s processes to arrive the claimed limitation since it was known in the art that the SEM is suitable for observing a by restricted field of vision at a high magnification.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh et al. (USP 6,900,135 hereinafter referred to as “Somekh”) in view of Shinada et al. (USP 6,329,826 hereinafter referred to as “Shinada”) and further in view of Branco et al. (USP 6,841,008 hereinafter referred to as “Branco”).

Somekh and Shinada disclose all the claimed limitations except for the cleaning comprises exposing the device feature to an oxygen containing plasma. Branco teaches that plasma cleaning with oxygen as a source gas (also referred to “ashing”) can remove organic based materials. At the same time, an oxygen plasma etch can leave quartz surfaces essentially unaltered as set forth in column 4, line 64-column 5, line 1). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use oxygen plasma for cleaning or etching, as taught by Branco since it was known in the art that oxygen plasma can remove organic based materials, and can leave quartz surfaces essentially unaltered.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh et al. (USP 6,900,135 hereinafter referred to as “Somekh”) in view of Shinada et al. (USP 6,329,826 hereinafter referred to as “Shinada”) and further in view of Kim et al. (USP 6,355,516 hereinafter referred to as “Kim”).

Somekh and Shinada disclose all the claimed limitations except for the device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer. Kim teaches in Fig. 1C that a device feature comprises a first conductive layer 12 located over a substrate 11, a buffer layer 13, 14, 15, 16 located over the first conductive layer, and a second conductive layer 17 located over the buffer layer (col. 2, line 40-col. 3, line 14). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first

Art Unit: 2818

conductive layer, and a second conductive layer located over the buffer layer, as taught by Kim in order to form a device feature as a capacitor.

Claim **23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh et al. (USP 6,900,135 hereinafter referred to as “Somekh”) in view of Shinada et al. (USP 6,329,826 hereinafter referred to as “Shinada”) and in view of Pike (USP 6,410,927), and further in view of Iwabuchi et al. (USP 6,512,227 hereinafter referred to as “Iwabuchi”).

Somekh, Shinada and Pike disclose all the claimed limitations except for at least one of the first and second inspections performed by a scanning electron microscope (SEM). Iwabuchi teaches that as one of apparatuses for observing a sample with an electron beam, there is known a scanning electron microscope (SEM). The SEM is suitable for observing a by restricted field of vision at a high magnification (col. 1, lines 32-39). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to use at least one of the first and second inspections is performed by a scanning electron microscope (SEM), as taught by Iwabuchi to incorporate into Somekh, Shinada and Pike’s processes to arrive the claimed limitation since it was known in the art that the SEM is suitable for observing a by restricted field of vision at a high magnification.

Claim **24** is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh et al. (USP 6,900,135 hereinafter referred to as “Somekh”) in view of Shinada et al. (USP 6,329,826

Art Unit: 2818

hereinafter referred to as “Shinada”) and in view of Pike (USP 6,410,927), and further in view of Branco et al. (USP 6,841,008 hereinafter referred to as “Branco”).

Somekh, Shinada and Pike disclose all the claimed limitations except for the cleaning comprises exposing the device feature to an oxygen containing plasma. Branco teaches that plasma cleaning with oxygen as a source gas (also referred to “ashing”) can remove organic based materials. At the same time, an oxygen plasma etch can leave quartz surfaces essentially unaltered as set forth in column 4, line 64-column 5, line 1). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use oxygen plasma for cleaning or etching, as taught by Branco since it was known in the art that oxygen plasma can remove organic based materials, and can leave quartz surfaces essentially unaltered.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh et al. (USP 6,900,135 hereinafter referred to as “Somekh”) in view of Shinada et al. (USP 6,329,826 hereinafter referred to as “Shinada”) and in view of Pike (USP 6,410,927), and further in view of Kim et al. (USP 6,355,516 hereinafter referred to as “Kim”).

Somekh, Shinada and Pike disclose all the claimed limitations except for the device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer. Kim teaches in Fig. 1C that a device feature comprises a first conductive layer 12 located over a substrate 11, a buffer layer 13, 14, 15, 16 located over the first conductive layer, and a second conductive

Art Unit: 2818

layer 17 located over the buffer layer (col. 2, line 40-col. 3, line 14). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer, as taught by Kim in order to form a device feature as a capacitor.

Allowable Subject Matter

Claims 7-9 are allowed.

Conclusion

Applicants' amendment necessitated the new ground(s) of rejection presented in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh whose telephone number is (703) 305-0089. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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Andy Huynh
Patent Examiner